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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/729,865	12/05/2003	En-Hsing Chen	023-0029	8494

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EXAMINER	
NGUYEN, VAN THU T	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 01/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/729,865	CHEN ET AL.	
	Examiner	Art Unit	
	VanThu Nguyen	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-60* is/are pending in the application.

4a) Of the above claim(s) *2-20,22,23 and 29-60* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 21, 24-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 12/12/05; 8/29/05; 6/10/05; 5/31/05; 3/21/05; 9/23/04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Claims 2-20, 22-23, 29-60 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected Groups and Species, there being no allowable generic or linking claim. Election was made without traverse in the reply filed on December 12, 2005.

2. Group I, Species 3 being pending claims 1, 21, 24-28 are present for examination.

Claim Rejections - 35 USC § 112

3. Claims 1, 21, 24-28 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, line 4, it not clear what it means by "of like type". Do Applicants mean to say the plurality of series selection devices comprises modifiable conductance as the memory cells? Same confusion applied for claim 25, line 2.

In claim 25, lines 1-3, it is not clear what apparently means in "wherein each NAND string includes a second plurality of series selection device of the like at the second end thereof". There is no "a first plurality of series selection device" in the previous claims.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an

international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1, 21, 24, 27-28 are rejected under 35 U.S.C. 102(b)/(e) as being anticipated by Sakui et al. (U.S. Patent No. 6,411,548, referring hereafter as Sakui) or Scheuerlein et al. (P.G. Pubs 2004/0125629, referring hereafter as Scheuerlein).

Regarding claim 1, Sakui discloses an integrated circuit comprising a memory array (see FIG. 48) including memory cells arranged in a plurality of series-connected NAND strings (see FIG. 47 for example of one NAND string), said memory cells comprising modifiable conductance switch devices (MONOS EEPROM cells, see column 42, line 7), said NAND strings including at a first end thereof a respective plurality of series selection devices (select gate transistor S2, see FIG. 47).

Regarding claim 21, Sakui also discloses wherein each NAND string includes at least one series selection device at a second end thereof opposite the first end (select gate transistor S1, see FIG. 47).

Regarding claim 24, Sakui discloses wherein pairs of NAND strings (e.g. one NAND string of BLOCK a connected to BL1 and one NAND string of BLOCK b connected to BL1, see FIG. 48) are arranged so that the respective second end connect of each string of the pair is coupled to a respective global array line (inherent select gate transistors S1(s) having control inputs signals SSLa and SSLb, which are connected bit line BL1, see FIG. 48); and the respective first end of each string of the pair is coupled to a shared bias node (inherent select gate transistors S2(s) having control input signals GSLa and GSLb, which are connected to bias voltage of SL, see FIG. 48).

Regarding claim 27, Sakui also discloses series selection devices having a charge storage dielectric (select gate transistors S1(s) having block insulating films 40SSL between the control gate 27SSL and charge storing layer 26SSL, see FIG. 44).

Regarding claim 28, Sakui further discloses series selection devices are maintained by periodic programming biasing to a higher threshold voltage than fabricated (see FIGS. 52-53).

Regarding claims 1, 21, 24-28, see entire disclosure of Scheuerlein, e.g. FIGS. 1-3.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 25-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakui in view of Chen et al. (U.S. Patent No. 6,266,275, referring hereafter as Chen) or Ichige et al. (P.G. Pubs. No. 2004/0152262, referring hereafter as Ichige).

Sakui discloses, as applied in prior rejection of claim 21, all claimed limitations except further limitation as set forth in claim 25.

Regarding claim 25, Chen discloses, in FIG. 4, a NAND string 401 having first end connected to a gate transistor 416, second end connected to series gate transistors 403 and 404. Ichige also discloses, in FIG. 50, a NAND string having first end connected to three series gate transistors and second end connected to other three series gate transistors.

Since Sakui and Chen/Ichige are all from the same field of endeavor, the purpose disclosed by Chen/Ichige would have been recognized in the pertinent art of Sakui.

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to have two gate transistors connect in series at one end of a NAND string memory for the purpose of improving programming efficiency.

Regarding claim 26, Sakui also discloses a pair of NAND strings (e.g. first NAND string of BLOCK a connected to BL1, and second NAND string of BLOCK b connected to BL1, see FIG. 48) are arranged so that:

a first group of control signals (SSLb, GSLa) couples the respective second end of one string of the pair to a global array line associated with the pair (second NAND string of BLOCK b being coupled to BL1 via control signal SSLb), and couples the respective first end of the other string of the pair to a respective bias node (first NAND string of BLOCK a being coupled to source line SL supplying bias voltage via control signal GSLa); and

a second group of control signals (SSLa, GSLb) couples the respective first end of said one string of the pair to a respective bias node (second NAND string of BLOCK b being coupled to source line SL supplying bias voltage via GSLa), and couples the respective second end of the other string of the pair to the global array line associated with the pair (first NAND string of BLOCK a being coupled to BL1 via control signal SSLa).

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to VanThu Nguyen whose telephone number is (571) 272-1881. The examiner can normally be reached on Monday-Friday, 9:00am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

January 7, 2006

VanThu Nguyen
Primary Examiner
Art Unit 2824